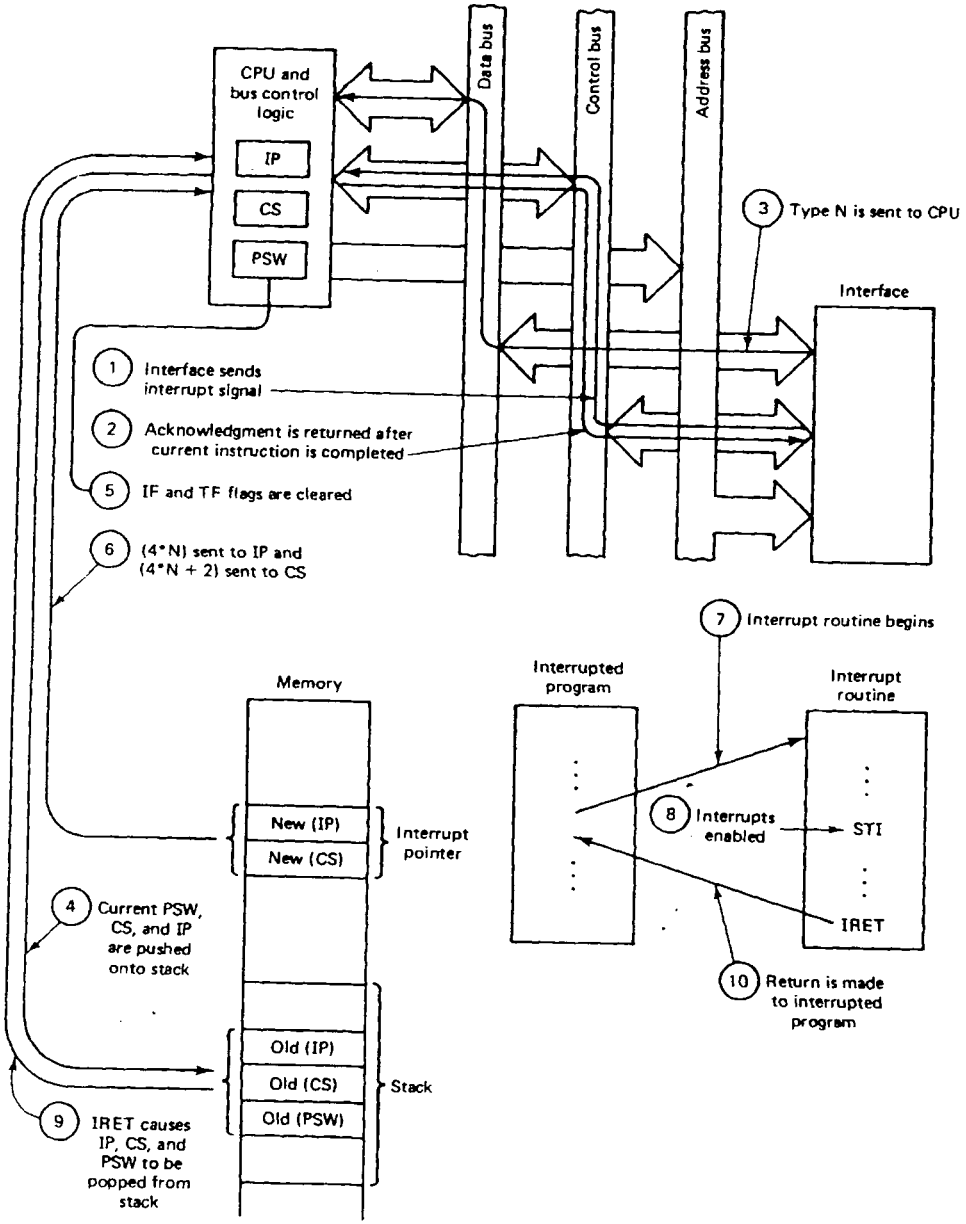

Figure 6-9 Sequence of events during a maskable interrupt and subsequent return.

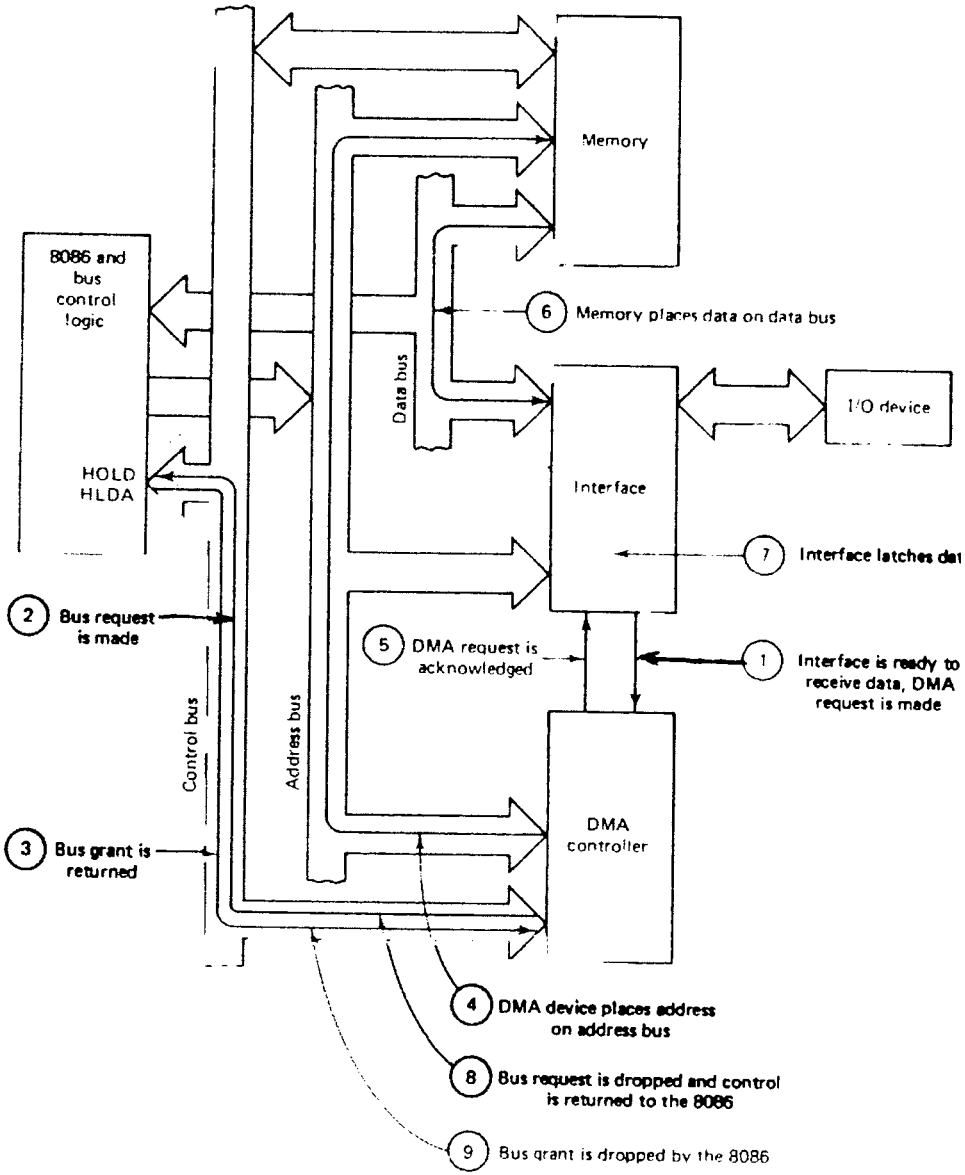

Figure 6-16 Single datum output transfer during a block transfer.